A unit for and method of video signal enhancement and image display apparatus provided with such a video signal enhancement unit

The invention relates to a video signal enhancement unit comprising:

- a pixel counter for generating a count of pixels representative of the number of pixels that occur within a predetermined period of time and which have video signal levels that are higher than a predetermined video level, and
- a processing unit for modifying contrast of the video signal in dependence on the count of pixels.

The invention further relates to an image display apparatus provided with:

- receiving means for receiving a video signal;
- a display device for displaying images represented by the video signal; and
- a video signal enhancement unit comprising:
- a pixel counter for generating a count of pixels representative of the number of pixels that occur within a predetermined period of time and which have video signal levels that are higher than a predetermined video level, and
- a processing unit for modifying contrast of the video signal in dependence on the pixel count.

The invention further relates to a method of video signal enhancement comprising:

- a first step to generate a count of pixels representative of the number of pixels that occur within a predetermined period of time and which have video signal levels that are higher than a predetermined video level; and
- a second step to modify contrast of the video signal in dependence on the count of pixels.

A unit of the kind described in the opening paragraph is known from United States Patent 5,422,680.

In this unit the amplitude range of the picture signal can be divided into a number of histogram segments, whereafter it is determined by means of a measurement per

histogram segment how often a pixel value or how long the picture signal occurs with an amplitude in the relevant histogram segment. Subsequently, the picture signal is processed by a non-linear unit having a transfer characteristic which is based on the integral of the histogram: per histogram segment the picture signal is amplified by a factor which depends on the contents of the relevant measured histogram segment.

A drawback of the unit is that it requires relatively many elements per histogram segment, i.e. pixels, in order to determine an accurate transfer characteristic. This results in a delay of at least one field. Other disadvantages of this unit are its complexity and its costs. Analyzing the video signal, storing several intermediate results, i.e. a histogram, and calculating a transfer characteristic based the histogram requires relatively many components.

It is a first object of the invention to provide a video signal enhancement unit of the kind described in the opening paragraph that has a relatively fast time response.

It is a second object of the invention to provide an image display apparatus comprising such a video signal enhancement unit.

It is a third object of the invention to provide a method of video signal enhancement of the kind described in the opening paragraph resulting in a relatively fast time response.

The first object of the invention is achieved in that the video signal enhancement unit is characterized in that the predetermined period of time, during which the count of pixels is determined, is a number of times shorter than one video field interval.

Because this predetermined period of time is relatively short the pixel counter can already start to generate control pulses for contrast modification after having analyzed only a portion of a video field. The latency is less than one video field. The video signal is taken to the desired level in a period of time that is hardly noticeable by the observer of the images, represented by the video signal. In the prior art a longer period of time is used in order to have more data to control the processing, which might be more accurate. Another advantage of the video signal enhancement unit according to the invention is that it can be made with relatively few, e.g. standard components like an EPLD (Erasable Programmable Logic Device).

An embodiment of the video signal enhancement unit according to the invention comprising:

- a contrast counter designed to provide control input for the processing unit and for storing a contrast count that is decreased each time the count of pixels exceeds a predefined threshold; and connected to the contrast counter

- a trigger means designed to generate a pulse, resulting in an increase of the contrast count.

The contrast counter is a kind of integrator that stabilizes the contrast modifications to apply. The current state of the video signal enhancement unit is based on results from previous analyses of pixel values and on previous contrast increase pulses. The transition to a next state is based on the current state and on the analyses of pixel values as performed in the last predetermined period of time or on the most recent contrast increase pulse.

In an embodiment of the video signal enhancement unit according to the invention, comprising a contrast counter and trigger means the trigger means is arranged to generate a pulse every video field. The trigger means generates contrast increase pulses independent from the operation of the pixel counter. The result is that the two controls, i.e. pixel counter for contrast decrease and trigger means for contrast increase, are de-correlated. The trigger means generates contrast increase pulses synchronized with the displaying of video fields. The frequencies of displaying fields and generating contrast increase pulses are mutual equal.

Another embodiment of the video signal enhancement unit according to the invention is characterized in further comprising a second pixel counter for generating a second count of pixels representative of a second number of pixels that occur within a second predetermined period of time and which have video signal levels that are higher than a second predetermined video level, and characterized in that the trigger means is arranged to generate the pulse if on a predetermined moment of time, the second count of pixels is less than a second predefined threshold. The generation of contrast increase pulses is determined by the second pixel count. That means that the generation of contrast increase pulses is conditional. Typically the second predetermined video level is less than the predetermined video level, e.g. 5-10 % less. Based on comparing the second count of pixels with the second predefined threshold, it is decided whether a contrast increase pulse should be generated. The result is a kind of hysteresis in the function describing the control of the contrast based on the video signal levels: the contrast is decreased if the count of pixels is higher than the predetermined threshold, the contrast is increased if the second count of pixels is less than the second predetermined threshold and the contrast remains unchanged if it appears that no

contrast change is required. The second predetermined period of time might correspond to the frequency of displaying fields. That means that during a field, the second count of pixels is determined. An advantage of this embodiment according to the invention is that a relatively stable control of contrast is achieved. This is particular of interest in the case of interlaced video. In that case it is possible that corresponding fields of one frame as received, differ in video signal level that much that different amounts of contrast enhancement could be applied, causing a flicker. With this embodiment of the video signal enhancement unit according to the invention the contrast of both fields of one frame will be enhanced substantially equal.

An embodiment of the video signal enhancement unit according to the invention comprises, coupled to the contrast counter, a contrast comparator to limit the contrast count to a maximum contrast value. To prevent saturation of cathodes or blooming on Cathode Ray Tubes (CRTs) or even overloading of power supplies the video signal should not be amplified too much. In the case of Plasma Display Panels (PDPs) a too much amplified video signal can result in clipping, i.e. pixels are displaying the maximum possible luminance value.

In an embodiment of the video signal enhancement unit according to the invention the maximum contrast value is controllable. This embodiment comprises means to control the maximum amplification, i.e. contrast modification. It might be that the various users of the video signal enhancement unit have different preferences concerning optimal video enhancement.

An embodiment of the video signal enhancement unit according to the invention comprises a contrast comparator that controls the trigger means to stop generating pulses when the contrast count has reached the controllable maximum contrast value. When the contrast count has reached that level, it is of no use to continue with generating pulses.

The second object of the invention is achieved in that the image display apparatus is provided with a video signal enhancement unit being characterized in that the predetermined period of time, during which the count of pixels is determined, is a number of times shorter than one video field interval.

The third object of the invention is achieved in that with the method of video signal enhancement the predetermined period of time, during which the count of pixels is determined, is a number of times shorter than one video field interval.

These and other aspects of the video signal enhancement unit and of the image display apparatus according to the invention will become apparent from and will be elucidated with reference with respect to the implementations and embodiments described hereinafter and with reference to the accompanying drawings, wherein:

Fig. 1 schematically shows an embodiment of the video signal enhancement unit; and

Fig. 2 shows elements of an image display apparatus.

Fig. 1 schematically shows an embodiment of the video signal enhancement unit 100. The video signal enhancement unit 100 comprises:

- a pixel counter 104 for generating a count of pixels representative of the number of pixels that occur within a predetermined period of time and which have video signal levels that are higher than a predetermined video level.
- a processing unit 102 for modifying contrast of the video signal in dependence on the count of pixels.
- a contrast counter 112 designed to provide control input for the processing unit 102 and for storing a contrast count that is decreased each time the count of pixels exceeds a predefined threshold.
- a trigger means 114 to generates a pulse in order to increase the contrast count.
- a contrast comparator 116 able to limit the contrast count to a maximum contrast value.

The data flow through and control signals of the signal enhancement unit 100 are described below. The video signal enters the video signal enhancement unit 100 at the input connector 120. The processing unit 102 multiplies the incoming video signal with a gain that is linearly related to the contrast count 126, that is between 1 and a controllable maximum contrast value, CM . The output of the video signal enhancement unit 100 is an enhanced video signal, i.e. with a modified contrast. The video signal enhancement unit 100 provides the output on the connector 122. The controllable maximum contrast value is stored in the contrast comparator 116, which can be optional, and can be adjusted via the input 118 of the contrast comparator 116. The video signal is analyzed by the pixel counter 104. The pixel counter 104 comprises a filter 106, an overflow detector 108 and an overflow counter 110. The filter 106 filters the video signal to extract only those parts from the video signal

that represent valid pixels. The overflow detector 108 detects whether the value of the current pixel exceeds a predefined pixel level threshold, PL_{th}, and generates a pulse each time that this occurs. The overflow counter 110 counts the pulses generated by the overflow detector 108. The overflow counter 110 holds the count of pixels. When the count of pixels exceeds a pre-selected count of pixels threshold, CP_{th}, the overflow counter 110 resets and gives a contrast decrease pulse 124 to the contrast counter 112. The contrast counter 112 holds the value of the contrast count 128, CC, and provides this value to the contrast comparator 116. So, every P pixels, with P larger than the count of pixels threshold, CP_{th}, with a pixel value higher than the pixel level threshold, PL_{th}, the contrast count, CC, is decreased. In pseudo language this can be expressed with:

$$\text{if } PL > PL_{th} \text{ then } CP := CP+1; \quad (1)$$

$$\text{if } CP > CP_{th} \text{ then } \{CC := CC-1;\ CP := 0;\} \quad (2)$$

The trigger means 114 is arranged to generate a contrast increase pulse 130 at the beginning of every video field. This contrast increase pulse 130 is consumed by the contrast counter 112, which adapts the contrast count 126 accordingly. In pseudo language this can be expressed with:

$$\text{if } (t == t0+k*T_{field}) \text{ then } CC := CC+DeltaC; \quad (3)$$

Note that the absolute value of the contrast increase, caused by a contrast increase pulse 130 might differ from the absolute value of the contrast decrease, caused by a contrast decrease pulse 124. In equation: $DeltaC \neq 1$.

When the contrast comparator 116 detects that the contrast count 128 is at the level of the controllable maximum contrast value, CM, then the contrast comparator 116 controls the trigger means 114 to stop generating contrast increase pulses 130. This control is arranged via connection 132 between the contrast comparator 116 and the trigger means 114. Expression 3 should be rewritten as:

$$\text{if } (t == t0+k*T_{field} \;\&\&\; CC < CM) \text{ then } CC := CC+DeltaC; \quad (4)$$

When the contrast count is below a predefined threshold, the contrast comparator 116 controls the trigger means 114 to start generating increase pulses 130 again.

The dynamic behavior of the video signal enhancement unit 100, i.e. the process of contrast modification can be explained with the following use-case. Suppose all pixels are below PL_{th}. Then the count of pixels will never exceed the count of pixels threshold, CP_{th}, and consequently the overflow counter 110 will never give a contrast decrease pulse 124 to the contrast counter 112. However, as long as the maximum contrast

value is not reached yet, every field, $t=t_0+k*T_{field}$, the trigger means 114 generates a contrast increase pulse 130. The result is that the contrast of the video signal is enhanced. This process of increasing the contrast continues until the level of the video signal, i.e. pixel levels, start exceeding the pixel level threshold, PL_{th}. Then the overflow detector 108 starts generating pulses, and eventually the overflow counter 110 will give contrast decrease pulses 124 to the contrast counter 112. At that moment the video signal enhancement unit 100 reaches the equilibrium state: the contrast decrease pulses in one field match the contrast increase pulse per field. Note that a contrast decrease pulse 124 will only be generated in case of overflow. It might be e.g. in the case of a dark scene and a low maximum contrast value that the pixel level threshold, PL_{th} is never exceeded.

Fig. 2 shows elements of an image display apparatus 200 according to the invention. The image display apparatus 200 has a receiving means 202 for receiving a video signal representing the images to be displayed. The signal may be a broadcast signal received via an antenna or cable but may also be a signal from a storage device like a VCR (Video Cassette Recorder) or DVD (Digital Versatile Disk). The data may be conform to a digital standard like DVI (Digital Visual Interface). The image display apparatus 200 further has a video signal enhancement unit 204 for processing the video signal and a display device 206 for displaying the images represented by the processed video signal. The video signal enhancement unit 204 is implemented as described in Fig. 1.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention and that those skilled in the art will be able to design alternative embodiments without departing from the scope of the appended claims. In the claims, any reference signs placed between parentheses shall not be constructed as limiting the claim. The word 'comprising' does not exclude the presence of elements or steps not listed in a claim. The word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. The invention can be implemented by means of hardware comprising several distinct elements and by means of a suitable programmed computer. In the unit claims enumerating several means, several of these means can be embodied by one and the same item of hardware.